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An Optimized Synchronous Techniques of Single Phase Enhanced Phase Locked Loop (EPLL)

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Abstract: *In applications of grid connected power converter, phase tracking is vital. An enhanced phase locked loop can be used to obtain magnitude and phase information of a positive sequence fundamental component of grid voltage. This paper presents the design; simulation and analysis of first and second order adaptive notch filter enhanced phase locked loop. The analysis of the phase tracking of enhanced phase locked loop has been done when the input signal is under normal operation condition or has disturbances. The results show that the second order adaptive notch filter design is able to produce a better synchronous signal in phase with the input signal under different operation conditions except under harmonics. In harmonics scenario, the second order adaptive notch filter based phase locked loop shows higher immunity compared with single phase adaptive notch filter phase locked loop.*

Keywords: *adaptive notch filter, enhanced phase looked loop, nonlinear filter, phase locked loop, second order ANF*

I. Introduction

Distributed Generation (DG) technologies have been experiencing a rapid integration into power systems, and they are expected to become more important in the future. However, the difference in the characteristics between these technologies and the system demand requires a conditioning system. In order to integrate these technologies in a conventional power system, power electronic converters play a vital role [1]. However, controlling a large number of DGs creates intimidating new challenges for operating and controlling the utility grid efficiently and reliably.

II. Objectives

The aim behind this work is:

- to design the first order adaptive filter base phase locked loop;
- to optimize the performance of phase locked loop using second order adaptive notch filter; and
- to simulate and analyze the performance of the first and second order adaptive notch filter based phase locked loop in the Matlab/Simulink computer environment.

III. Literature Review

Voltage source converters enable DG systems to be utilized as a dynamic voltage regulator through dynamic controlling of the voltage at the point of common coupling. Yet, they have more controlled variables compared with conventional generation technologies [2]. As a matter of fact, the fundamental phase angle of the utility voltage is a critical controlled variable for this kind of device. This angle is used to generate a reference signal in order to synchronize the operation condition of the distributed generation system with the utility grid. As a result, an accurate phase tracking method is needed to achieve the phase angle information of the grid.

Various methods were developed and can be classified into two approaches; an open loop tracking approach (such as low pass filters, Kalman method, and space vector method) and a closed loop approach such as a phase locked loop (PLL) [3].

PLL approach has been widely used in communication system, motor control systems and other industrial applications. In power system fields, this technique has been adopted to provide fast and accurate synchronization between the DG side and the utility. However, it is expected to be highly immune to disturbances such as harmonics, noises, sags, unbalances and other distortions.

The phase locked loop technique can be divided according to its structure into stationary reference (SR) frame based PLL, synchronously rotating reference frame (SRF) or zero crossing detection (ZCD) based PLL. The ZCD based PLL method is sensitive to frequency transient and distortion notch [4]. SR frame and SRF based PLLs do not work accurately during unbalance condition [5, 6]. Thus, the enhanced PLL (EPLL) has been adopted as it has a high degree of immunity to harmonic and unbalance conditions over conventional PLLs [7].

IV. Methodology

The operation principle of the EPLL is based on the conventional PLL, where it is accomplished through a phase detector (PD) and the positive-sequence fundamental phase component is estimated [8]. Then the output signal of the PD is filtered by a loop filter (LF) before entering a voltage controlled oscillator (VCO) where it is synchronized with the input signal as shown in Fig. 1. An adaptive filter (AF) works on the concept of the adaptive noise cancelling (ANC) concept, at which it adjusts its own parameters automatically. An adaptive notch filter (ANF) technique is used in EPLL to attenuate a specific range of frequencies of the input signal to enhance the performance of the PD of the conventional PLL.

Fig. 2 illustrates the main concept of ANF where the output of the VOC is applied to the PD as a reference signal.

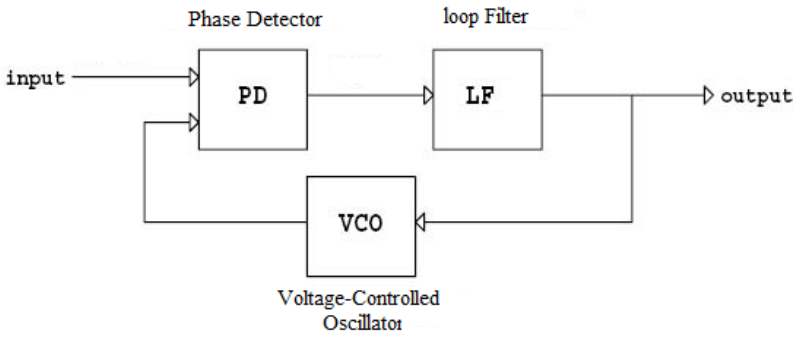


Figure 1. Block Diagram of a Basic Phase Locked Loop

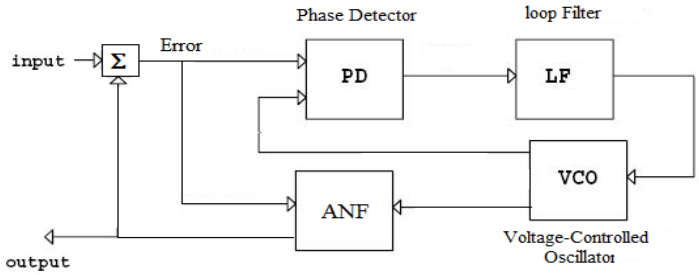


Figure 2. Block diagram of an enhanced phased locked loop with adaptive notch filter

In fact, PD causes a phase shift by 90º between the input phase signal and the reference phase signal. Yet, ANF generates zero-signal for the PD as the EPLL locked to the input signal. The design of EPLL can be optimized more by introducing a second order ANF which is built based on the ANC where the reference signal need to be filtered.

4.1. Design Description

The phase detector finds the difference between the input signal applied to the system and the output signal generated by VCO, which is known as the error. The output of PD has the double frequency ripple which can be partially removed using a loop filter. As a result, the LP bandwidth needs to be small in order to remove the double frequency ripple and other distortions, yet not too small that affects system response. Finally, the VCO changes its operating frequency when the error is not zero in order to generate the output signal at center frequency. Mathematically, based on [7], it can be interpreted as in equations (1), (2) and (3):

$$e(t) = v_{in}(t) - v_{out}(t) \quad (1)$$

$$v_{in}(t) = Vsin(\omega t + \varphi) \quad (2)$$

$$v_{out}(t) = Vsin(\omega t + \bar{\varphi}) \quad (3)$$

Where, $e(t)$ is the output signal of the PD, $v_{in}(t)$ is the input signal of EPLL, and $v_{out}(t)$ is the output signal of EPLL. It is clear that the error is a multivariable function of voltage magnitude, frequency and phase

angle. As a result, this error function needs to be minimized in the sense of the linear least square, as shown in equation (4).

$$E(V, \omega, \varphi) = \|v_{in}(t) - v_{out}(t)\|^2 \quad (4)$$

By using the method of steepest descent, the following three differential equations (5), (6) and (7) can be obtained:

$$\dot{v_{out}}(t) = Ke(t)\sin(\bar{\varphi}) \quad (5)$$

$$\dot{\bar{\omega}}(t) = K_i e(t)\cos(\bar{\varphi}) \quad (6)$$

$$\dot{\bar{\varphi}}(t) = \bar{\omega} + K_p e(t)\cos(\bar{\varphi}) \quad (7)$$

Where,K,K_i and K_p are step size constants. By using linear analysis [9] equation (5), (6) and (7) can be expanded to equations (8), (9) and (10):

$$\dot{v_{out}}(t) \approx \frac{K}{2}(V_{in} - V_{out}) \quad (8)$$

$$\dot{\bar{\omega}}(t) = \frac{K_i}{2} V_{in}(\varphi - \bar{\varphi}) \quad (9)$$

$$\dot{\bar{\varphi}}(t) = \bar{\omega} + \frac{K_p}{2} V_{in}(\varphi - \bar{\varphi}) \quad (10)$$

From these equations the approximated transfer function of the closed-loop system is given in equation (11):

$$G(s) = \frac{2\zeta\omega_n s + {\omega_n}^2}{s^2 + 2\zeta\omega_n s + {\omega_n}^2} \quad (11)$$

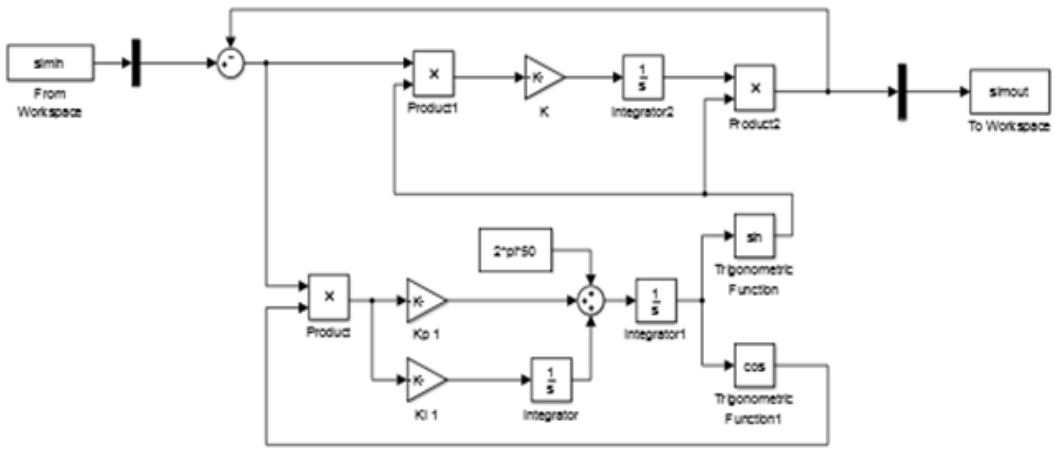
It is obvious that equation (11) is the second order which can give

$$\frac{K_p V}{2} = 2\zeta\omega_n \quad (12)$$

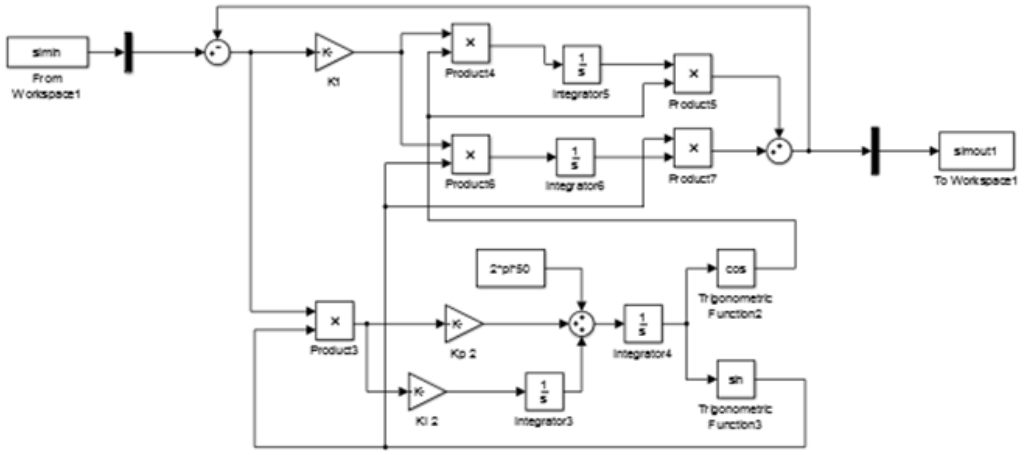
$$\frac{K_i V}{2} = {\omega_n}^2 \quad (13)$$

$$K = 2\zeta\omega_n \quad (14)$$

Where, ζ is damping ratio; which controls how fast the filter reaches its settle point and how much overshoot can have, ω_n is the natural frequency at no damp in (rad/s). Most of control systems, except of robotic control system, are design with damping factor $\zeta < 1$ to achieve high response speed consistent [10]. Thus, damping factor $\zeta = 0.7$ is chosen where at this value the system converges reasonably fast. Note that, natural frequency is $\omega_n = \frac{2\zeta}{\tau}$ where, τ is a time constant and is chosen to equal 2ms, and centered frequency is; $\omega_o = 2\pi \times 50$ rad/s, at which the output of the regulator is zero once the regulator has tracked the phase. The structure of EPLL is shown in Fig. 3.



(a)



(b)

Figure 3. Structure of Enhanced Phase Locked Loop in the Matlab/Simulink computer environment: (a) first order adaptive notch filter and (B) second order adaptive notch filter

To compare the two control systems, two indices are considered; the integration for the square of the error (ISE) and the integration for the absolute magnitude of the error (IAE) are given by:

$$ISE = \int_0^\infty e(t)^2 dt \quad (15)$$

$$ISE = \int_0^\infty |e(t)| dt \quad (16)$$

Therefore, the system with the minimum indices is considered the best control system.

V. Simulation Results

To test the performance of a fast and accurate synchronization of EPLL, it has been simulated in MATLAB under normal and grid fault conditions. During different fault scenarios the single phase voltage experience transients due to the appearance of voltage sags and frequency jump.

5.1. The EPLL Response Under Normal Operation Condition

During normal operation condition, a single phase voltage 1V p.u was applied to EPLL input with 50 Hz frequency. As shown in Fig. 4, the second order ANF based PL has much better response than conventional first order ANF based PLL. It detected the positive sequence components in about 1ms compared with the latter which locked the input signal after about 70ms. Fig. 5 illustates that second order ANF reaches steady state zero error much faster than conventional ANF with much less oscillations.

Table 1 depicts the integration error values for the first and second order ANF. It is obvious that ANF has higher ISE and IAE values, which indicate that second order has better response that first order ANF under normal operation condition.

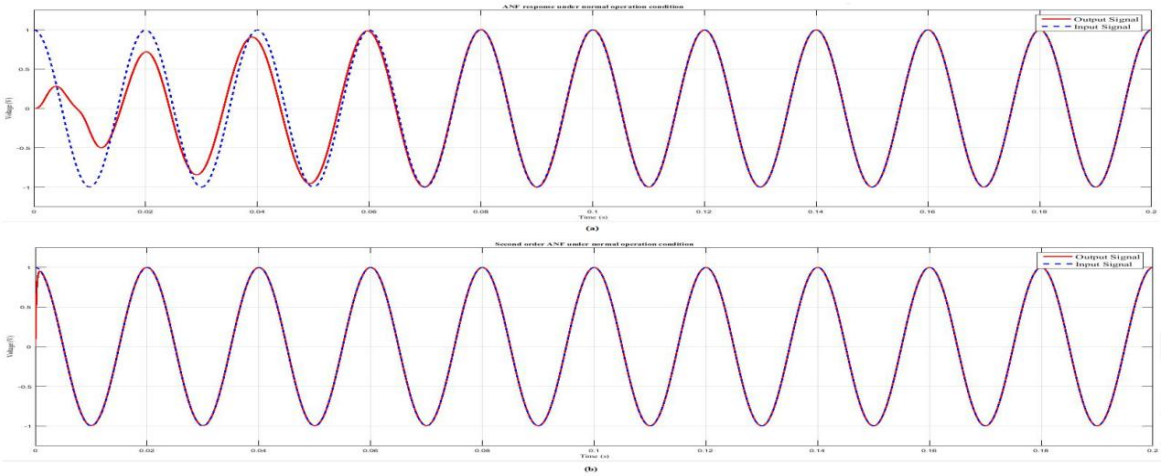


Figure 4. the EPLL response during normal operation condition: (a) first order adaptive notch filter, (b) second order adaptive notch filter

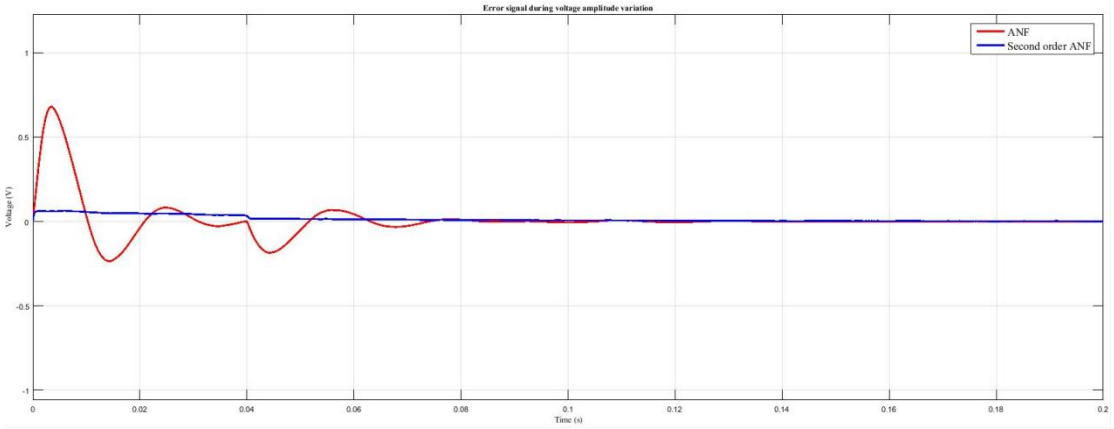


Figure 5. Error signal under normal operation condition

Table 1: The ISE and IAE for ANF and second order ANF, under normal operation condition

Error Signal	ANF	Second Order ANF
ISE (V)	0.00658	0.0000995
IAE (V)	0.0159	0.0004052

5.2. The EPLL Response Under Three Different Fault Conditions

Now, the performance of EPLL is simulatedfor different fault scenarios, as following;

5.2.1. *Scenario 1: voltage amplitude variation.*

Voltage sag is defined as reductions in the grid voltage, lasting from a cycle to milliseconds, which are caused by unexpected increases in loads such as faults, or by sudden increases in source impedance. In this scenario, voltage amplitude of input signal is reduced by 70 percent from its value after two cycles which gives a rise to high shortcircuit currents as illustrated in Fig. 6. During this scenario, the second order ANF output signal was able to lock with input signal after only 70ms. In contrast, the second order ANF based PLL locked the input signal after about 40ms. Moreover, the first order ANF based PLL responses with higher voltage amplitude than input voltage signal during the first cycle of the fault, as depicted by the arrows in Fig. 6 (a). Further, Fig. 7 depicts that once the second order ANF based PLL locked to the input signal, it keep locking even after voltage variation occur. While, in the first order ANF based PLL, the error signal experiences the oscillations after the fault occurs.

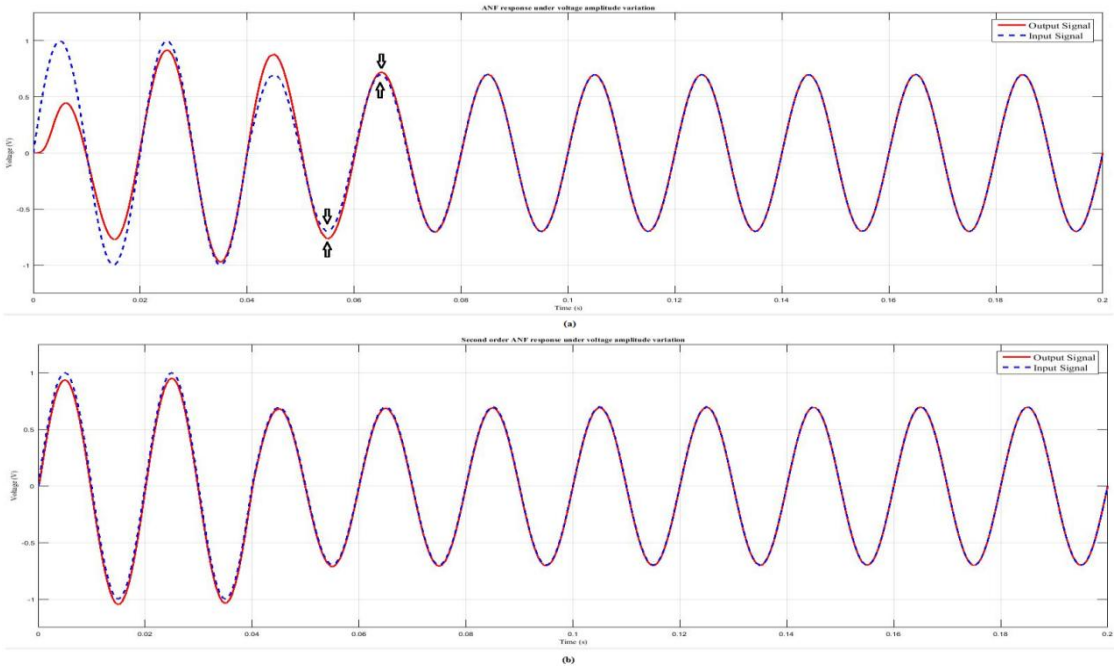


Figure 6. The EPLL Response During Voltage Amplitude Drop By 70 Percent: (A) ANF And (B) Second Order ANF

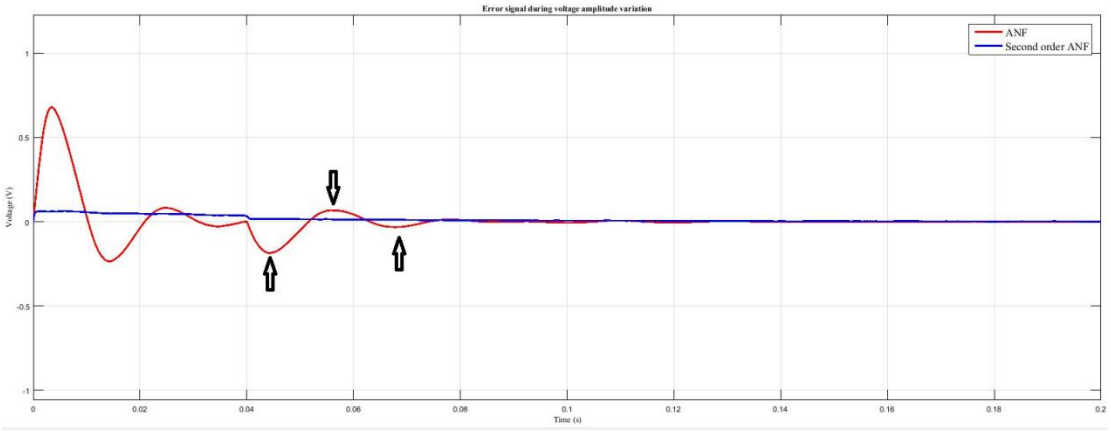


Figure 7. Error Signal Under Phase Fault with 70 Percent of The Reference Signal

Table 2 shows the integration error values for the first and second order ANF. It is clear that the second order ANF has better response than the first order ANF under voltage variation operation condition, where it has between 30 to 40 lower error indices, compared with first order ANF.

Table 2: The ISE and IAE for ANF and second order ANF, under voltage amplitude variation

Error Signal	ANF	Second Order ANF
ISE (V)	0.002701	0.0001058
IAE (V)	0.008694	0.002982

5.2.2. Scenario 2: Phase Jump

In this scenario, a phase jump occurs after about 86ms. In this kind of faults first order based EPLL shows that there is almost no immunity, where it is unlocked with the input reference signal after faults and it resynchronized again after three cycles and a half as illustrated in Fig.11.

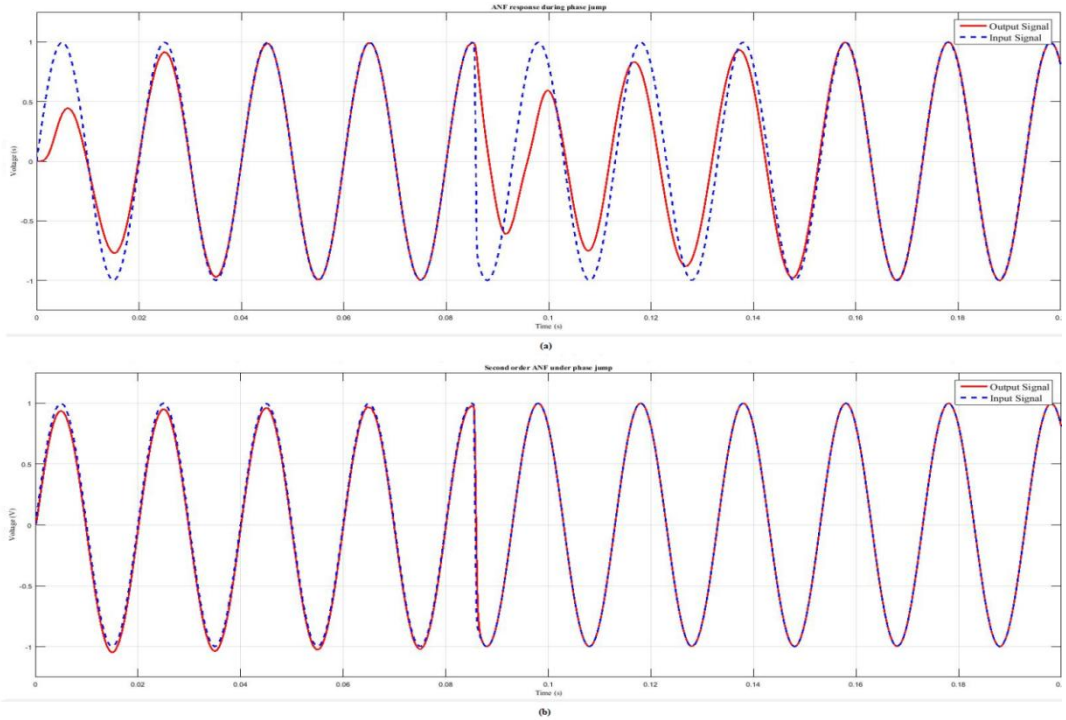


Figure 11. The EPLL output response for grid with phase jump; (a) ANF and (b) second order ANF

Fig. 12 depicts the error signal response of the two ANF techniques to the phase jump. Clearly, the first order ANF has a higher spike-shaped-error once the fault occurred and high oscillations to resynchronize.

Table 3 shows the ISE and IAE of two responses. In table 4, second order ANF shows also a faster response to phase jump much better than first order ANF.

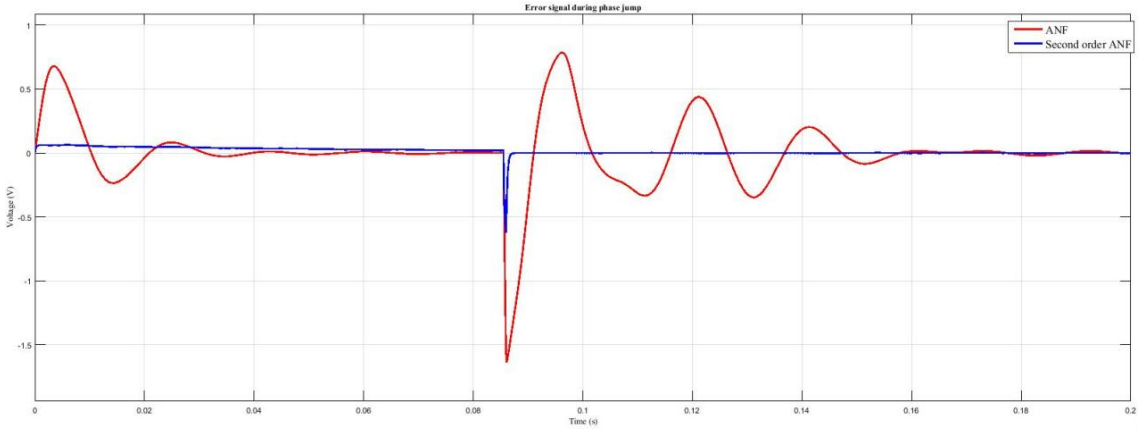


Figure 12. Error signal under for grid with phase jump

Table 3: The ISE and IAE for ANF and second order ANF, under phase jump

Error Signal	ANF	Second Order ANF
ISE (V)	0.01386	0.0002788
IAE (V)	0.0275	0.003573

VI. Conclusion

There are various methods of electrical phase synchronization have been proposed for the interconnection of distributed generation technologies with the national electrical grid. In this study, the adaptive notch filter are designed and analyzed. In addition, the enhanced phase locked loop is optimized using the second order adaptive notch filter in order to improve the speed of synchronization.

Both types have simple design configurations, as well as, the results demonstrate that the both EPLL design were able to track in phase with the input voltage signal under normal and various fault conditions. However, the second order ANF based PLL shows fast and accurate response, under normal and fault operation conditions much better than first order ANF based PLL.

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